

FIGURE 1 (Prior Art)

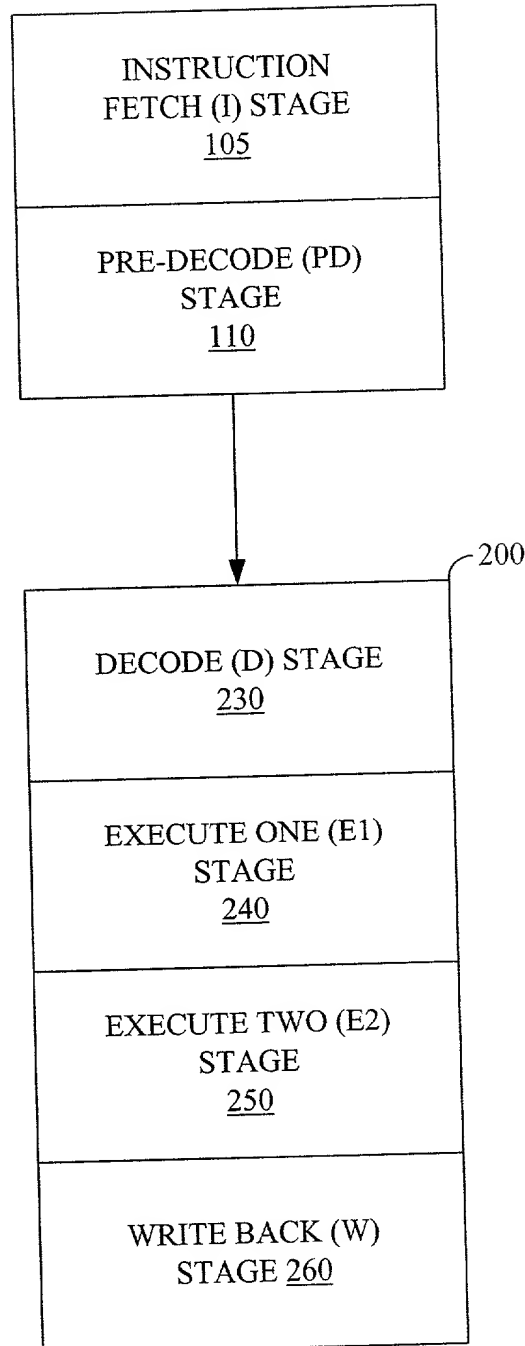


FIGURE 2 (Prior Art)

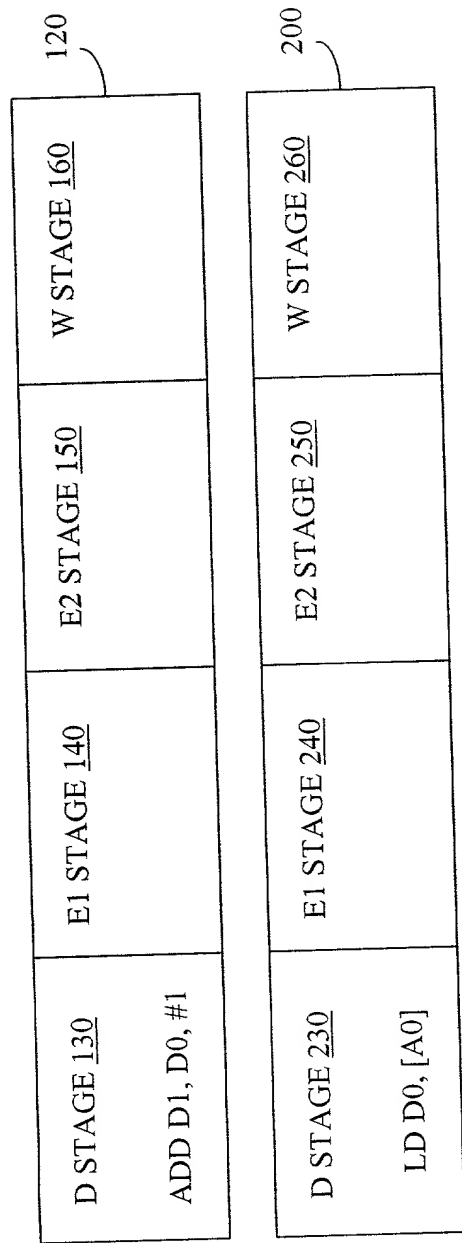


Figure 3(a)

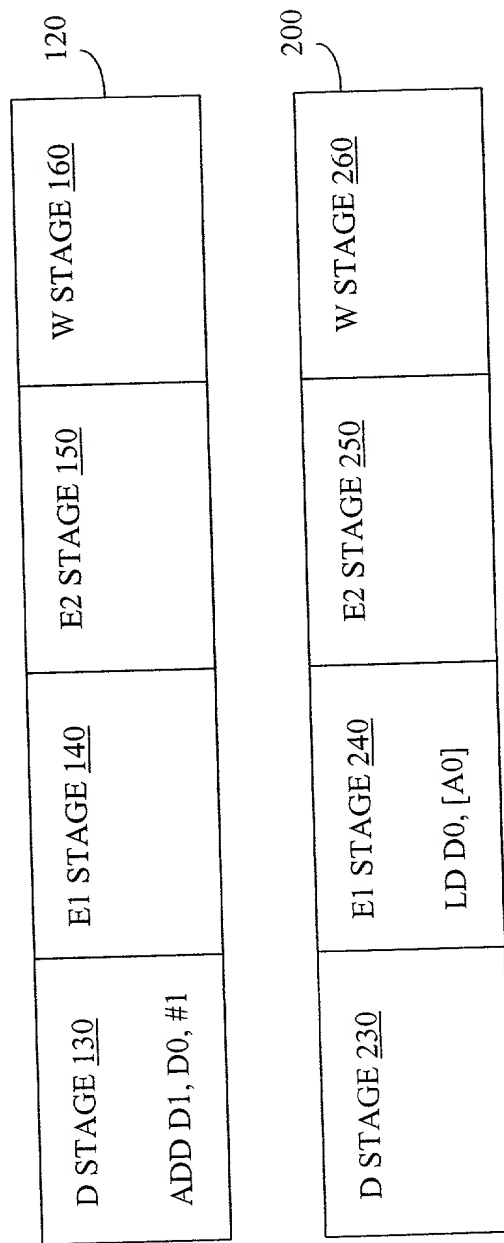


Figure 3(b)

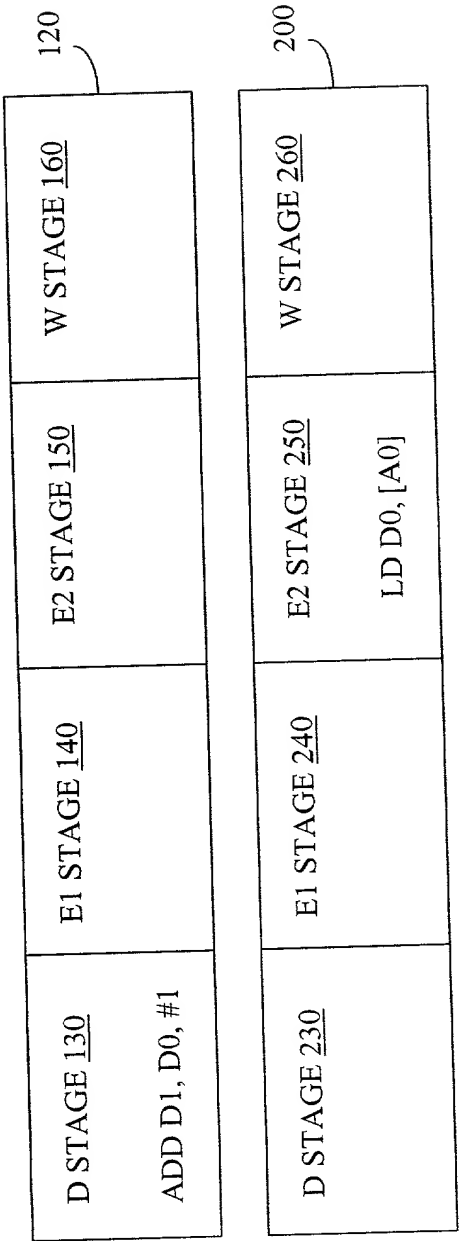


Figure 3(c)

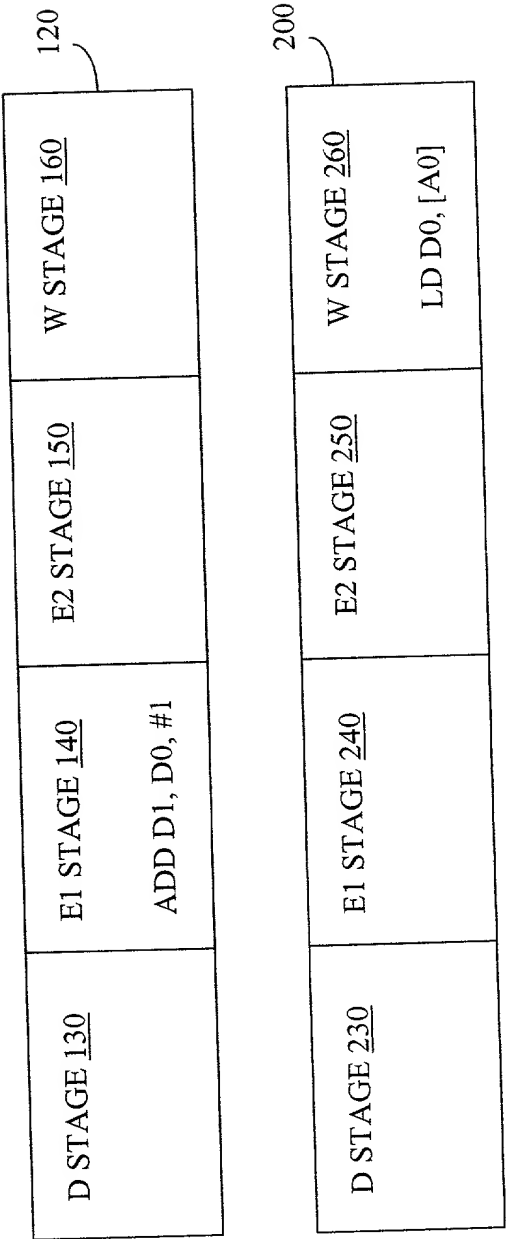


Figure 3(d)

FIG. 3(e) is a block diagram of a processor core 100, showing a pipeline with stages D, E1, E2, and W. The stages are labeled with their respective numbers: D STAGE 130, E1 STAGE 140, E2 STAGE 150, and W STAGE 160. The E2 stage is further labeled with the operation "ADD D1, D0, #1".

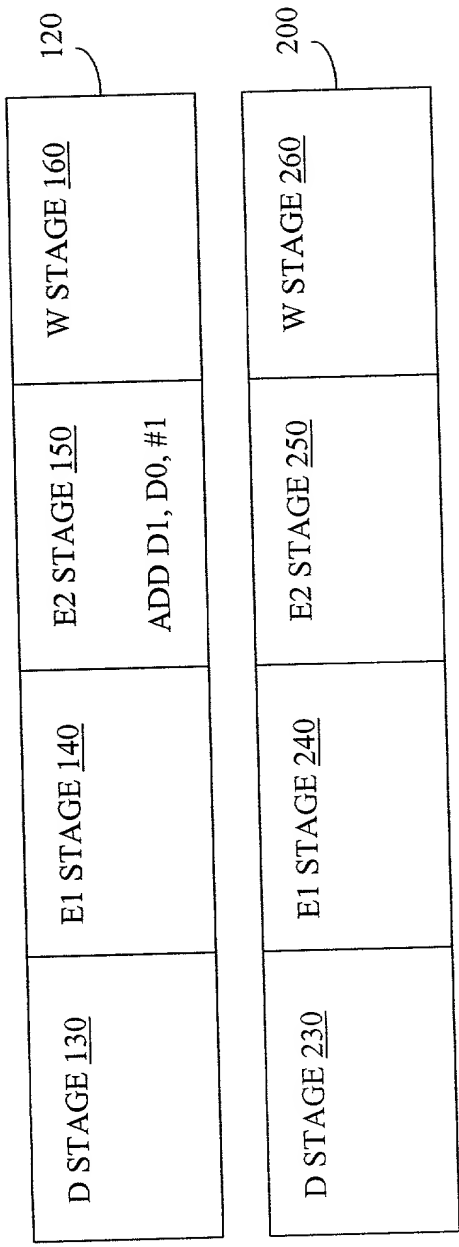


Figure 3(e)

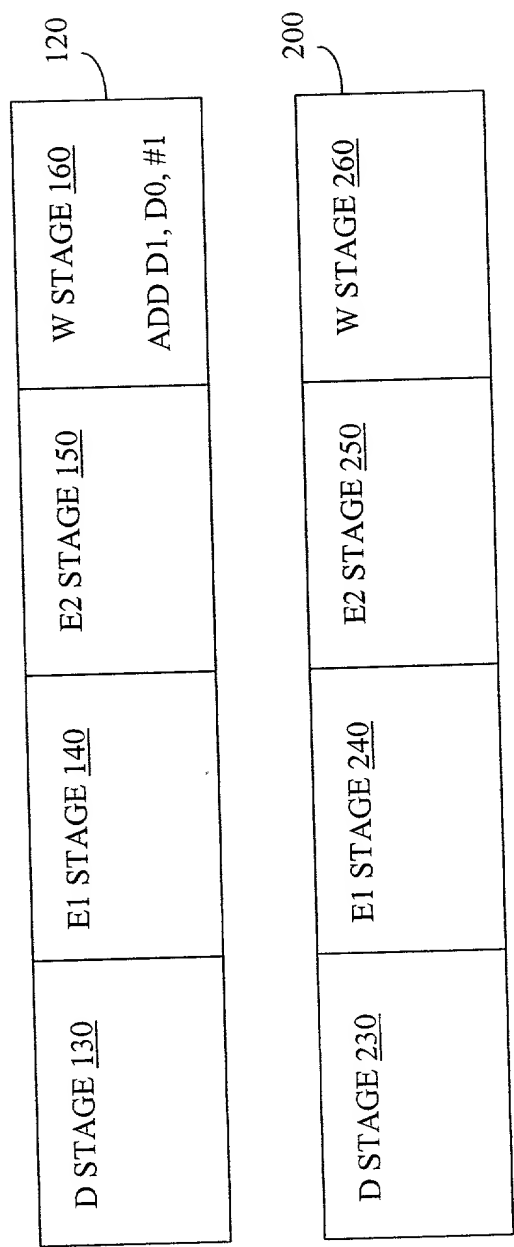


Figure 3(f)

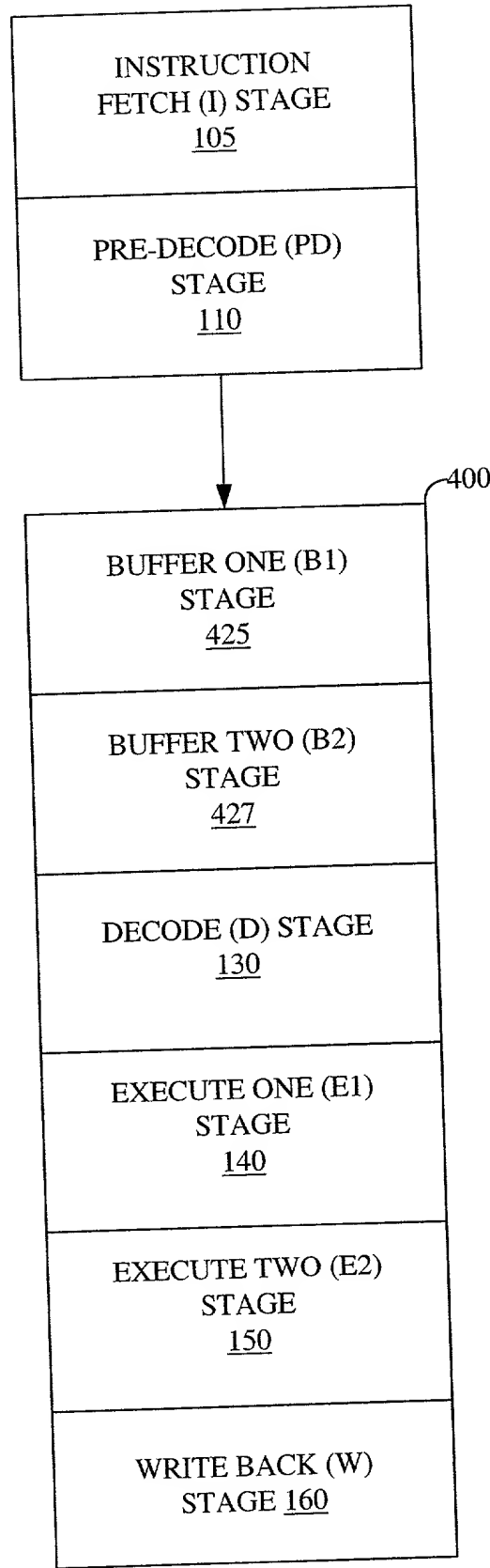


FIGURE 4 (Prior Art)

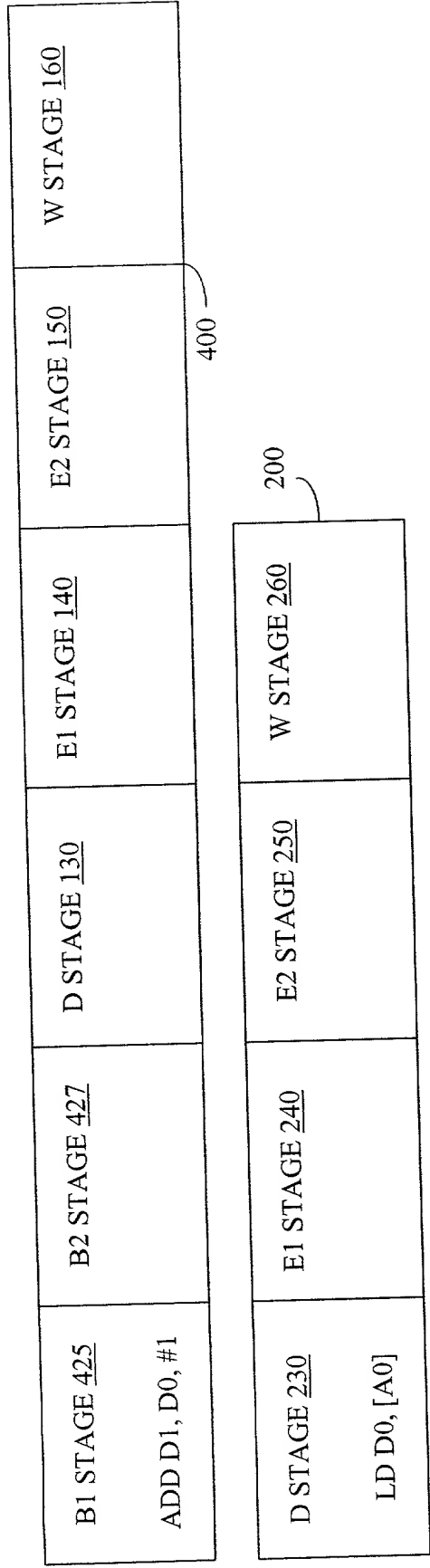


Figure 5(a)

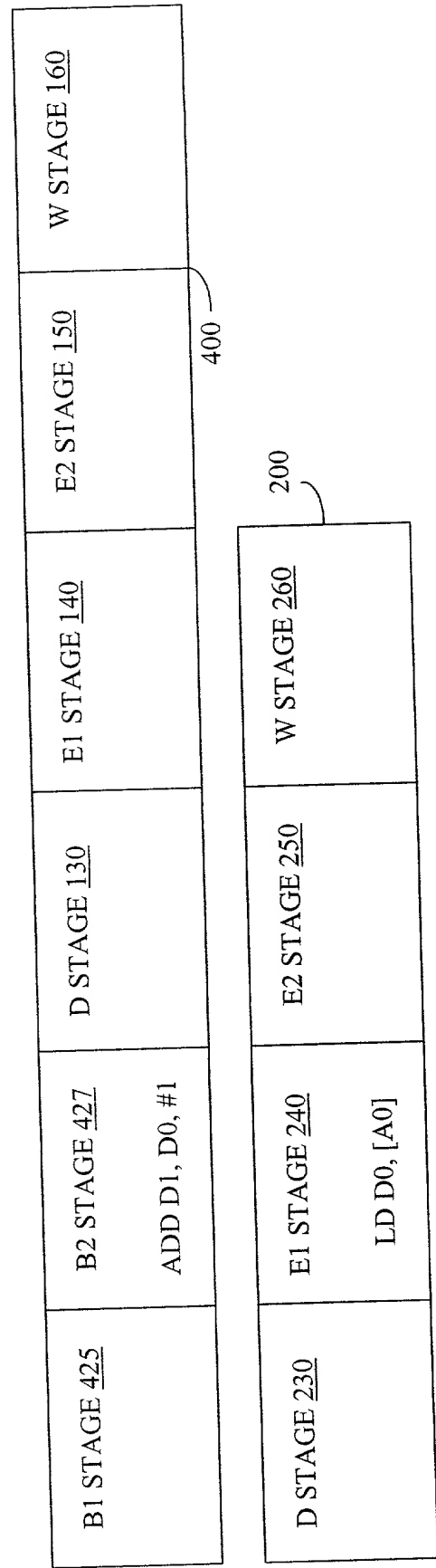


Figure 5(b)

FIG. 5(c) is a block diagram of a processor 400, according to one embodiment of the present invention. The processor 400 includes a B1 stage 425, a B2 stage 427, a D stage 430, an E1 stage 140, an E2 stage 150, and a W stage 160. The B1 stage 425 is connected to the B2 stage 427, which is connected to the D stage 430. The D stage 430 is connected to the E1 stage 140, which is connected to the E2 stage 150, which is connected to the W stage 160. The processor 400 is configured to execute instructions, such as ADD D1, D0, #1, LD D0, [A0], and ADD D1, D0, #1.

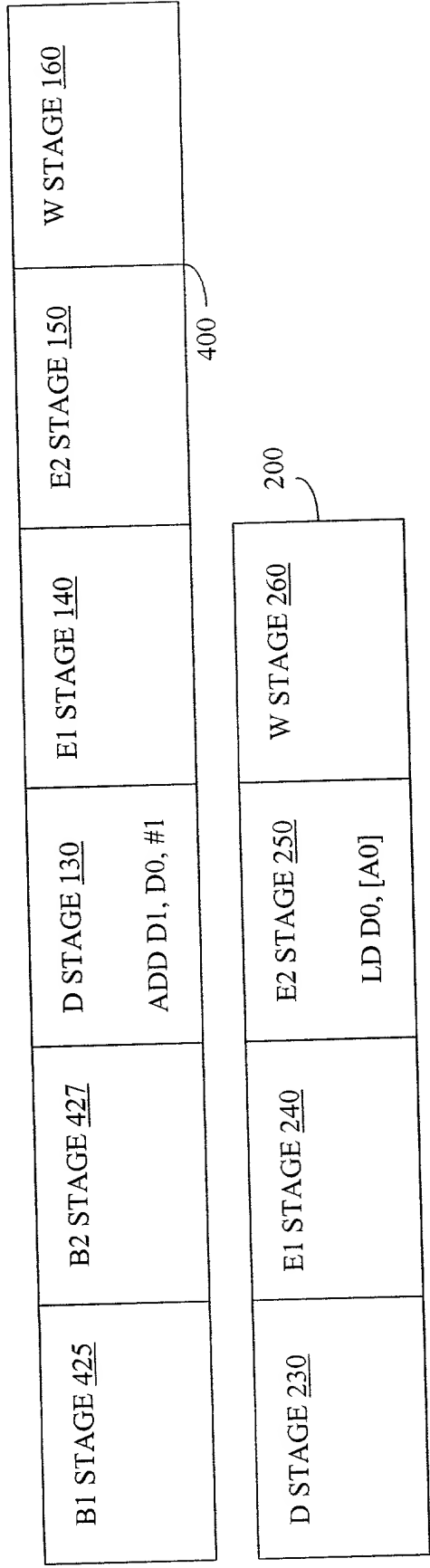


Figure 5(c)

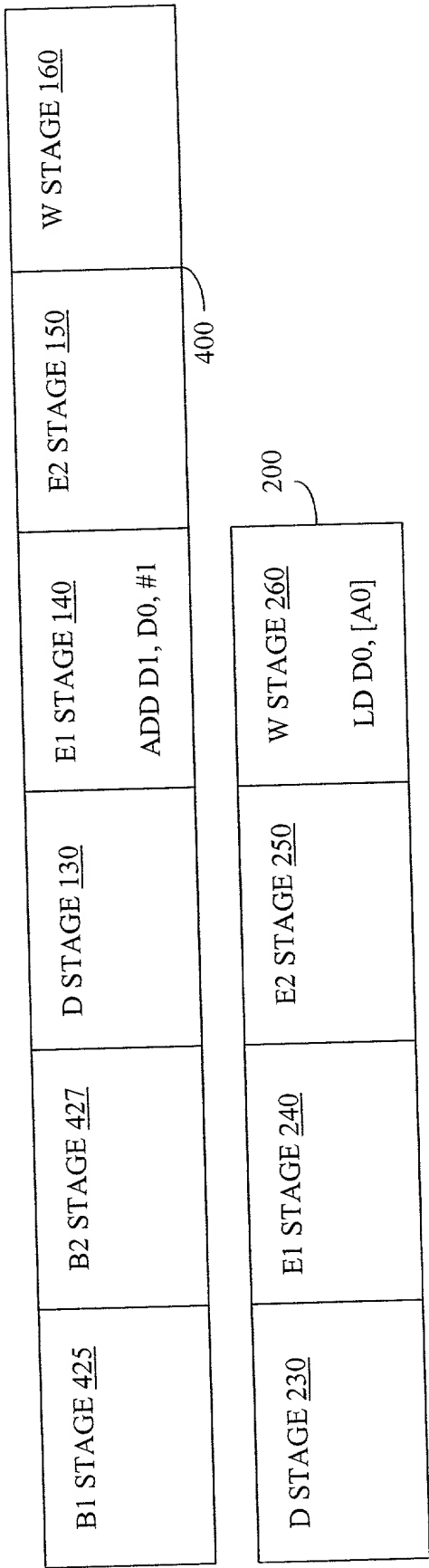


Figure 5(d)



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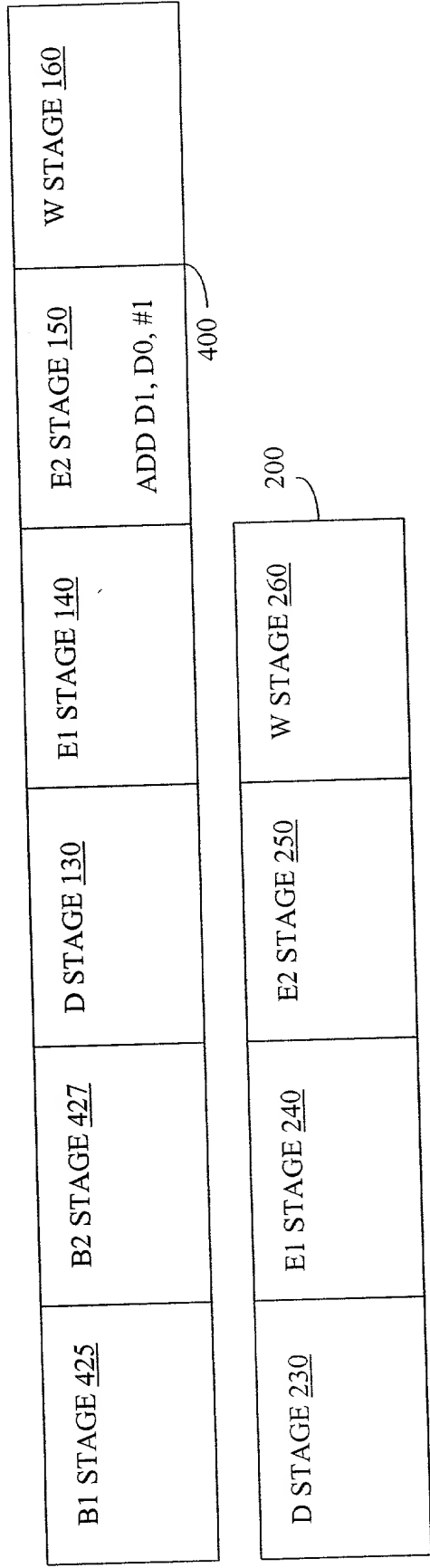


Figure 5(e)

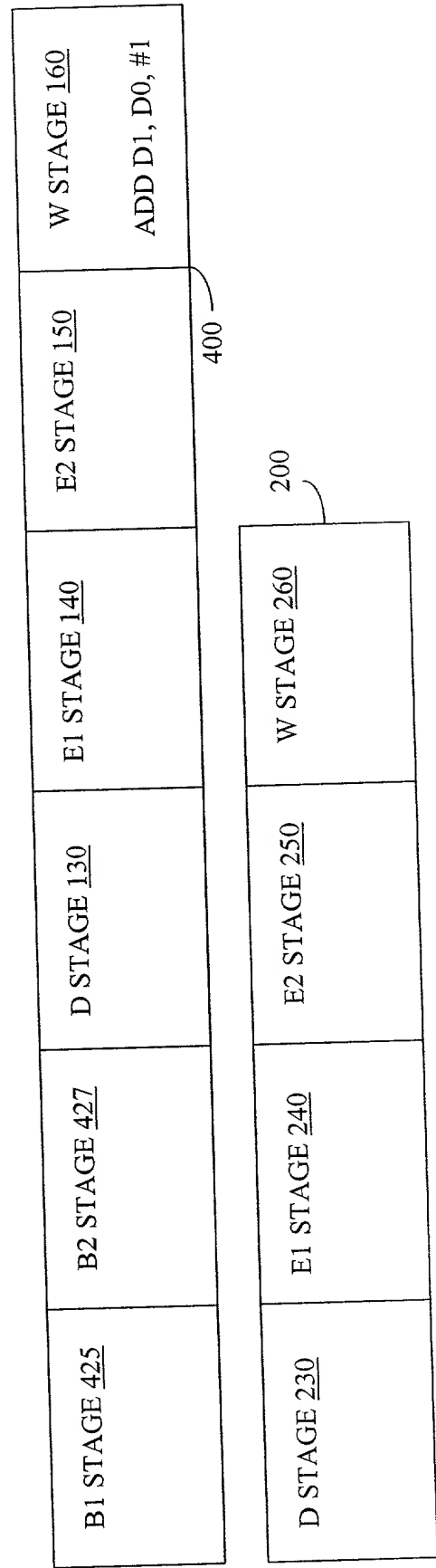


Figure 5(f)

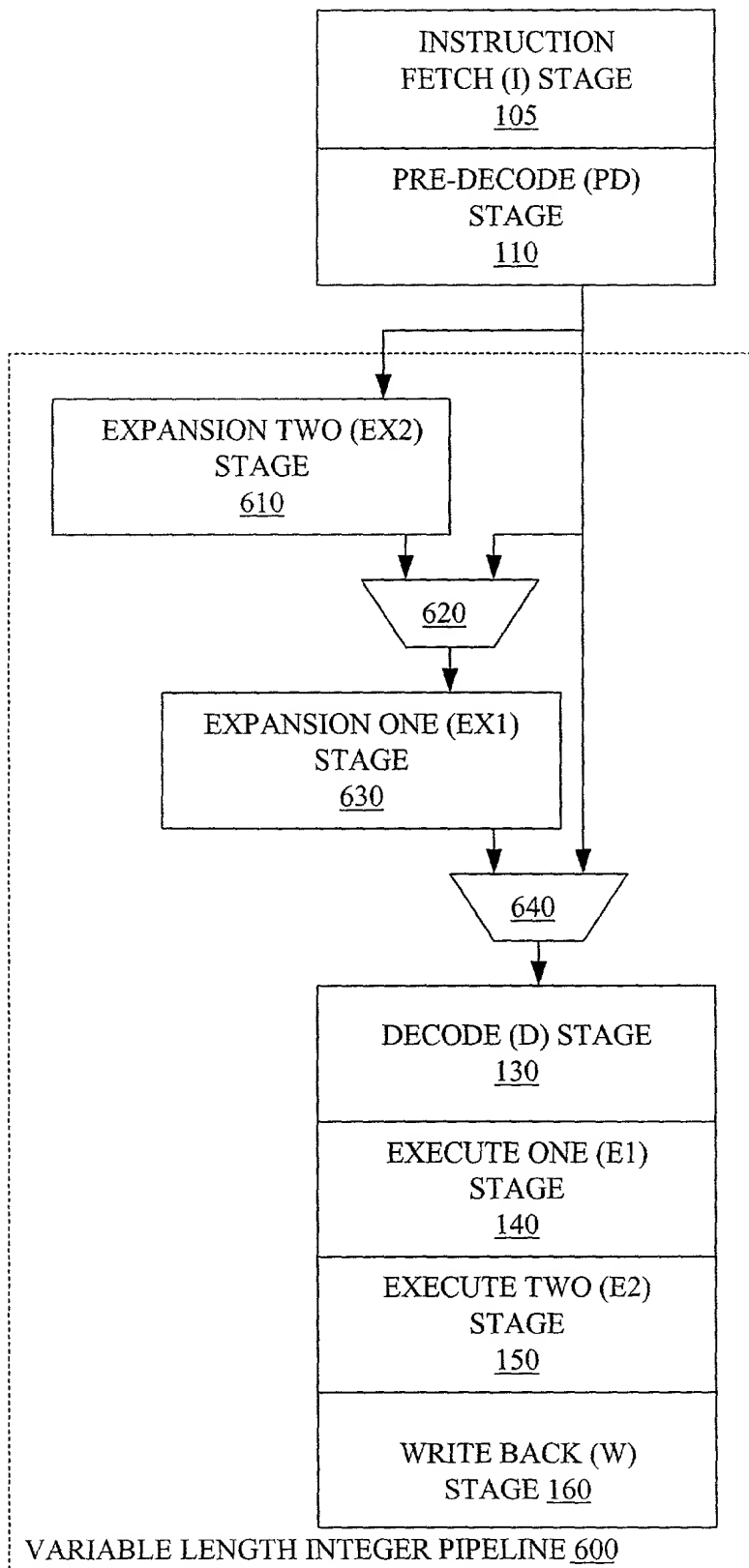


FIGURE 6

US 2017/0100000 A1  
FIG. 7(a)

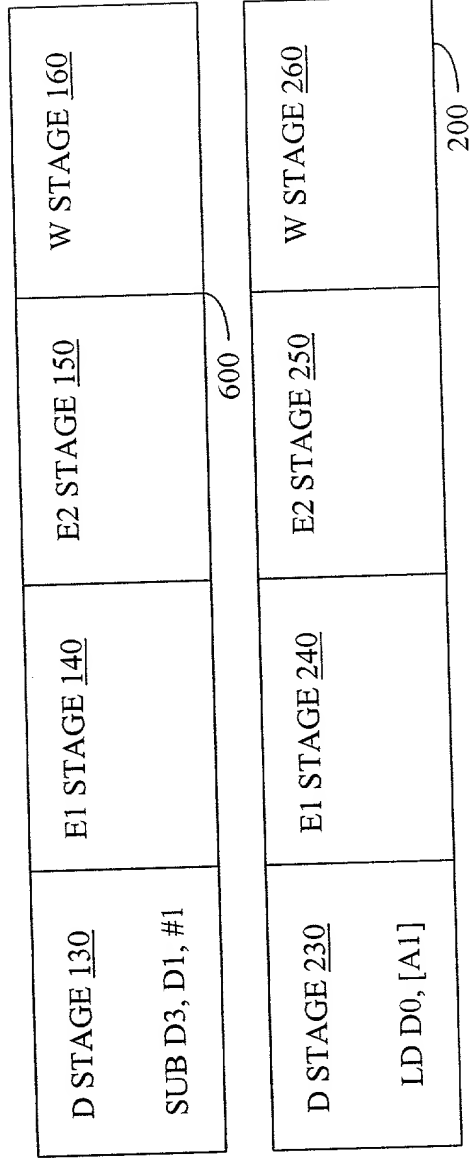


Figure 7(a)

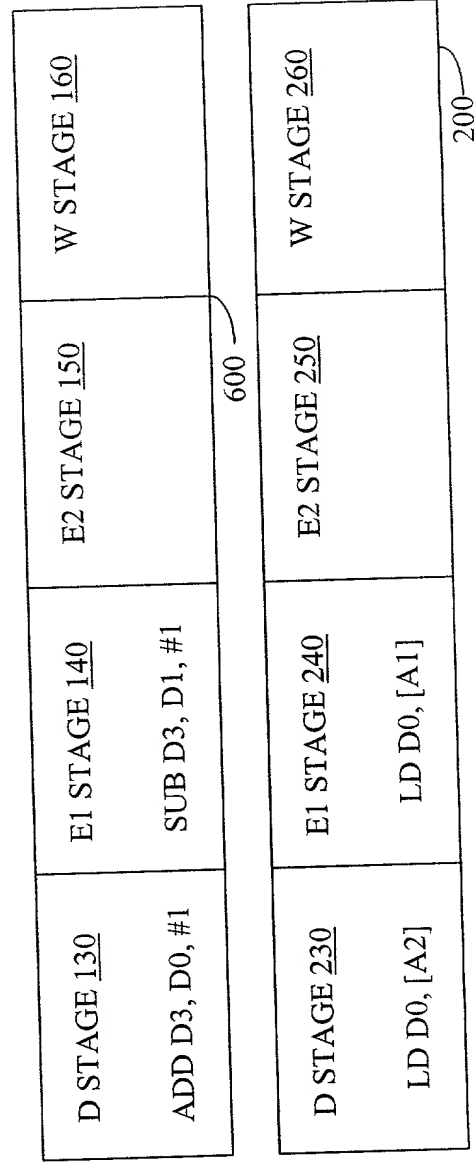


Figure 7(b)

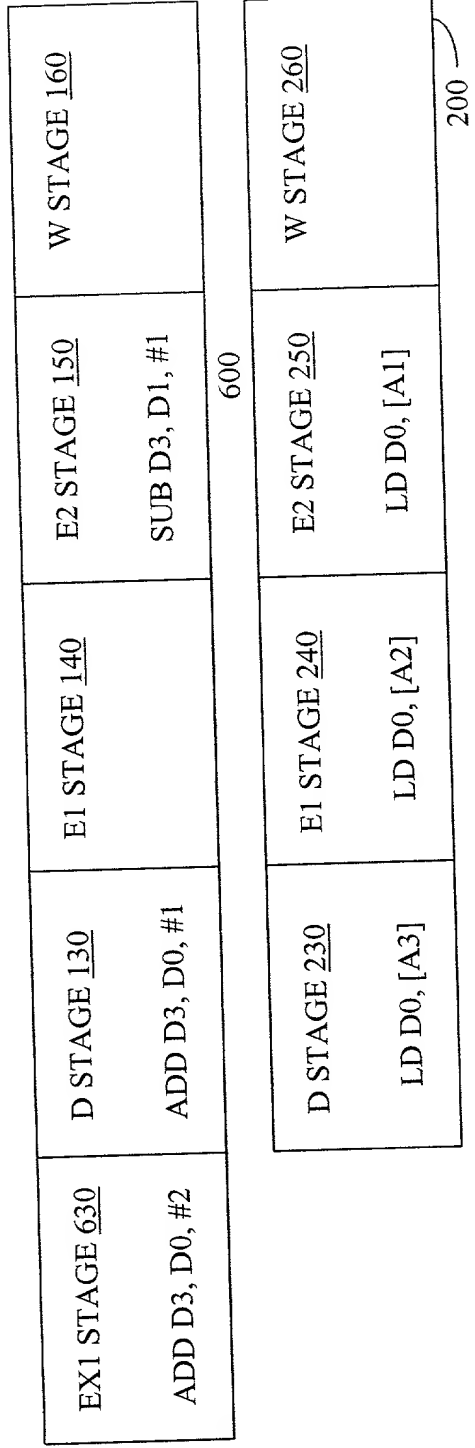


Figure 7(c)

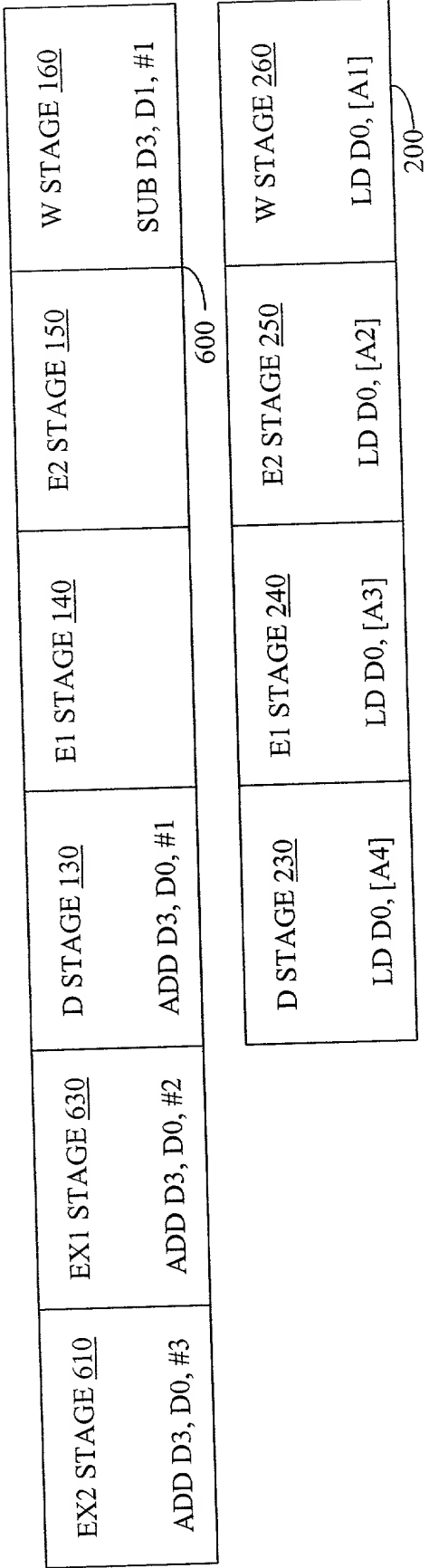


Figure 7(d)

FIG. 7(e) is a block diagram of a processor 200 showing a pipeline 600 with stages EX2, EX1, D, E1, E2, and W. The stages are connected in series, and the pipeline is labeled 600. The stages are: EX2 STAGE 610, EX1 STAGE 630, D STAGE 130, E1 STAGE 140, E2 STAGE 150, and W STAGE 160. The stages are connected in series, and the pipeline is labeled 600.

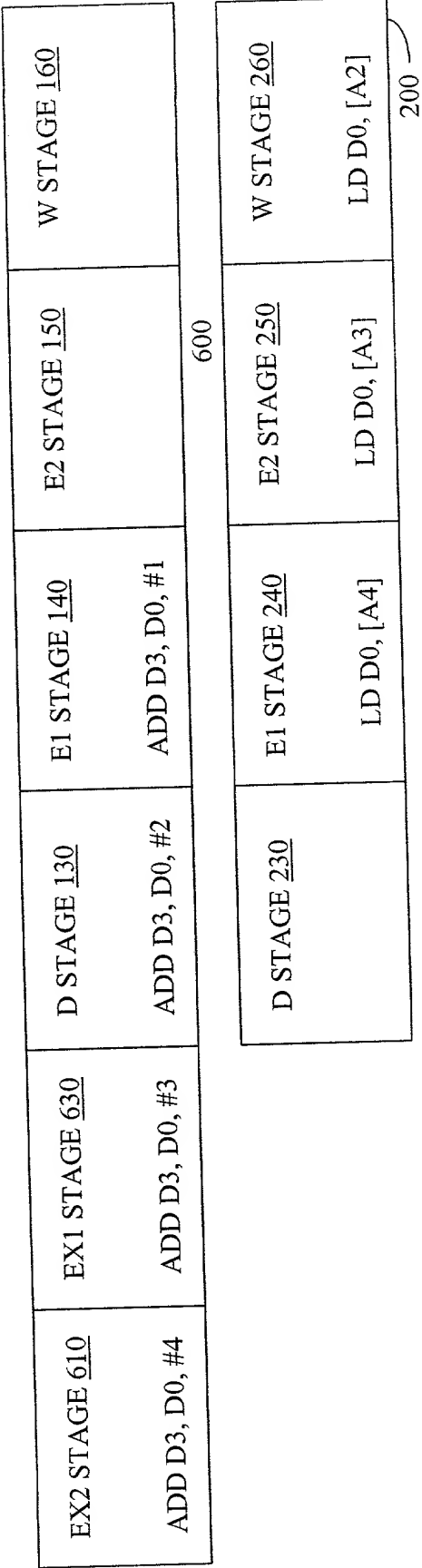


Figure 7(e)

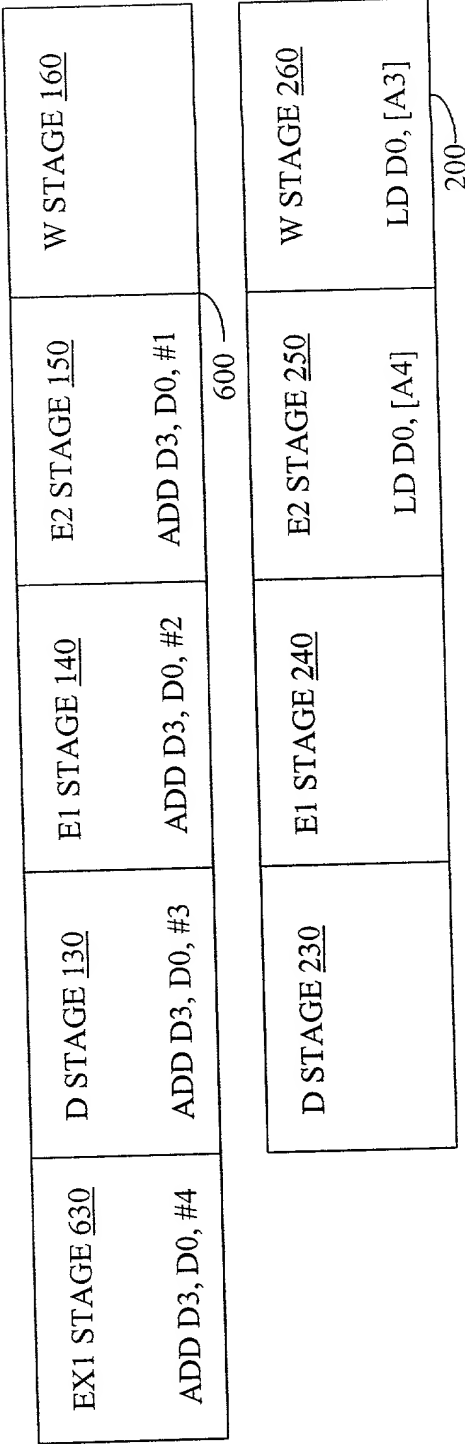


Figure 7(f)

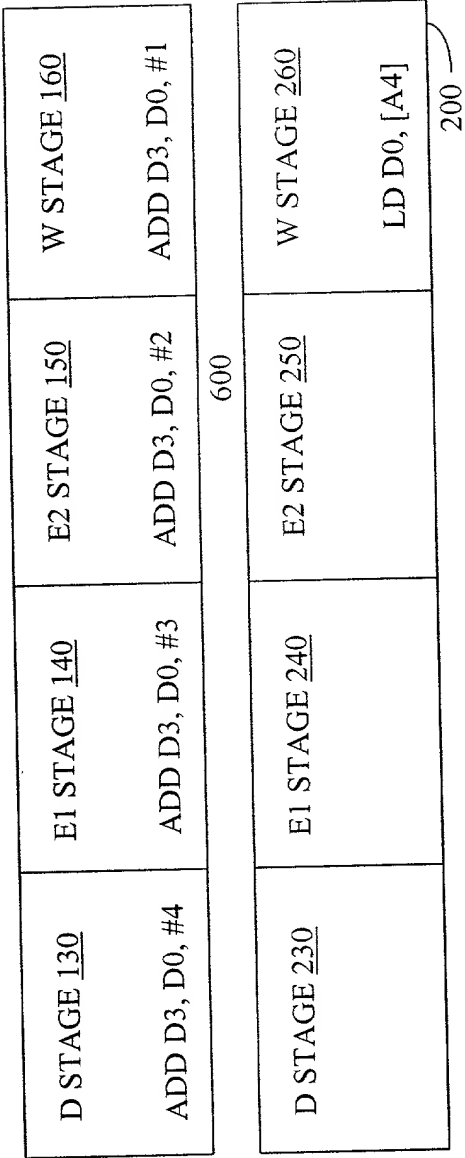


Figure 7(g)

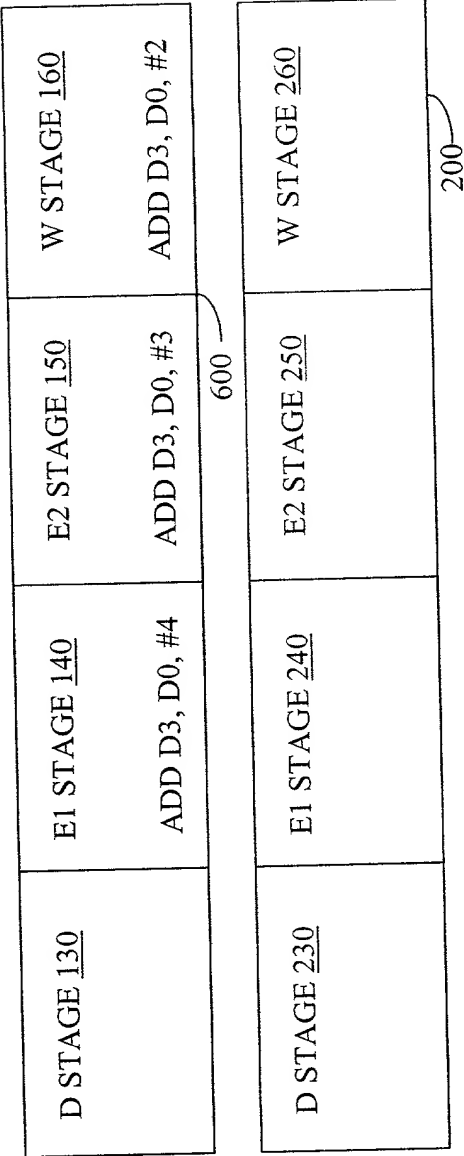


Figure 7(h)

FIG. 7(i) is a block diagram of a processing unit 200, which includes a D stage 130, an E1 stage 140, an E2 stage 150, and a W stage 160. The D stage 130 is connected to the E1 stage 140, which is connected to the E2 stage 150, which is connected to the W stage 160. The E2 stage 150 includes an adder 600 that adds D3, D0, and #4. The W stage 160 includes an adder 600 that adds D3, D0, and #3.

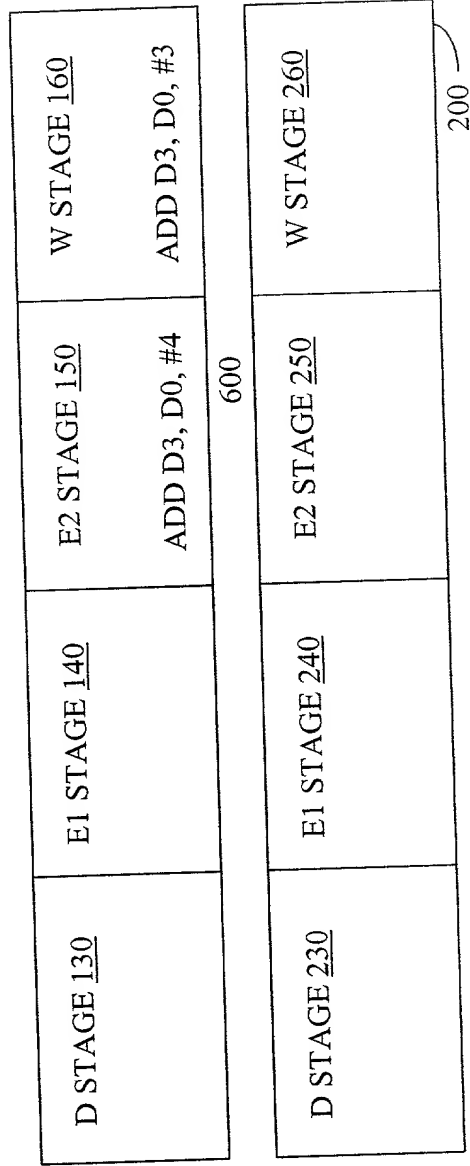


Figure 7(i)

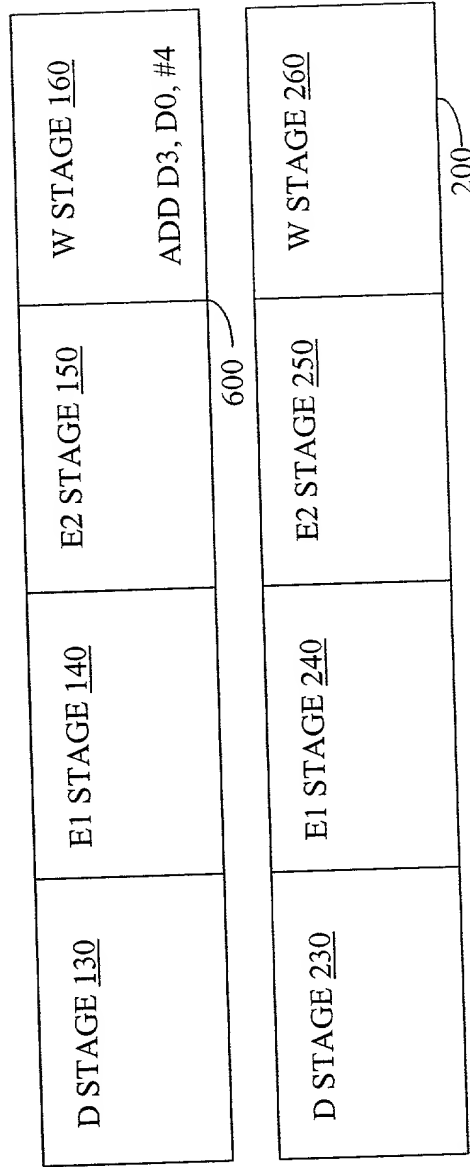


Figure 7(j)